Nagasaki et al. in view of Johnson et al. (U.S. Patent No. 6,351,406). These rejections are respectfully traversed.

Nagasaki does not disclose or suggest a ferroelectric memory device including, *inter alia*, a memory cell array and a peripheral circuit section disposed in different layers, as recited in claim 1.

Instead, Nagasaki discloses a peripheral circuit 6 disposed on the same layer as a memory cell array. See Fig. 2I of Nagasaki. Specifically, the common electrode 6 and the first electrode assembly 4 of Nagasaki are formed on the same surface of the substrate 2.

For at least these reasons, it is respectfully submitted that claim 1 is patentable over the applied references. The dependent claims are likewise patentable over the applied references for at least the reasons discussed as well as for the additional features they recite. Applicants respectfully request that the rejections under 35 U.S.C. 102 and 103 be withdrawn.

III. Conclusion

In view of the foregoing, Applicants respectfully submit that this application is in condition for allowance. Favorable consideration and prompt allowance are earnestly solicited.

Should the Examiner believe anything further is desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact Applicants' undersigned representative at the telephone number listed below.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

Benjamin M. Halpern
Registration No. 46,494

JAO/BMH:vgp

Date: May 13, 2003

OLIFF & BERRIDGE, PLC
P.O. Box 19928
Alexandria, Virginia 22320
Telephone: (703) 836-6400

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APPENDIX

Changes to Claims:

The following is a marked-up version of the amended claim:

1. (Amended) A ferroelectric memory device comprising:

a memory cell array in which memory cells are arranged in a matrix, the memory cell array including first signal electrodes, second signal electrodes arranged in a direction intersecting the first signal electrodes, and a ferroelectric layer disposed at least in intersection regions between the first signal electrodes and the second signal electrodes; and

a peripheral circuit section for selectively writing information into or reading information from the memory cell,

wherein the memory cell array and the peripheral circuit section are disposed in different layers, ~~and~~

wherein the peripheral circuit section is formed in a region outside the memory cell array, and

wherein the ferroelectric layer is disposed linearly along the first signal electrodes or the second signal electrodes.